FIG. 1

"A METHOD AND APPARATUS FOR PIPELINING ORDERED INPUT/OUTPUT TRANSACTIONS TO
COHERENT MEMORY IN A DISTRIBUTED MEMORY, CACHE COHERENT, MULTI-PROCESSOR SYSTEM"
by Manoj Khare, Akhilesh Kumar, Lily P. Looi
Docket No. P9301   Contact: Cynthia Thomas Faatz   Reg. No. 39,973   Phone No. 53-268-1442
Sheet 2 of 5
REPLACEMENT SHEET

FIG. 2

"A METHOD AND APPARATUS FOR PIPELINING ORDERED INPUT/OUTPUT TRANSACTIONS TO
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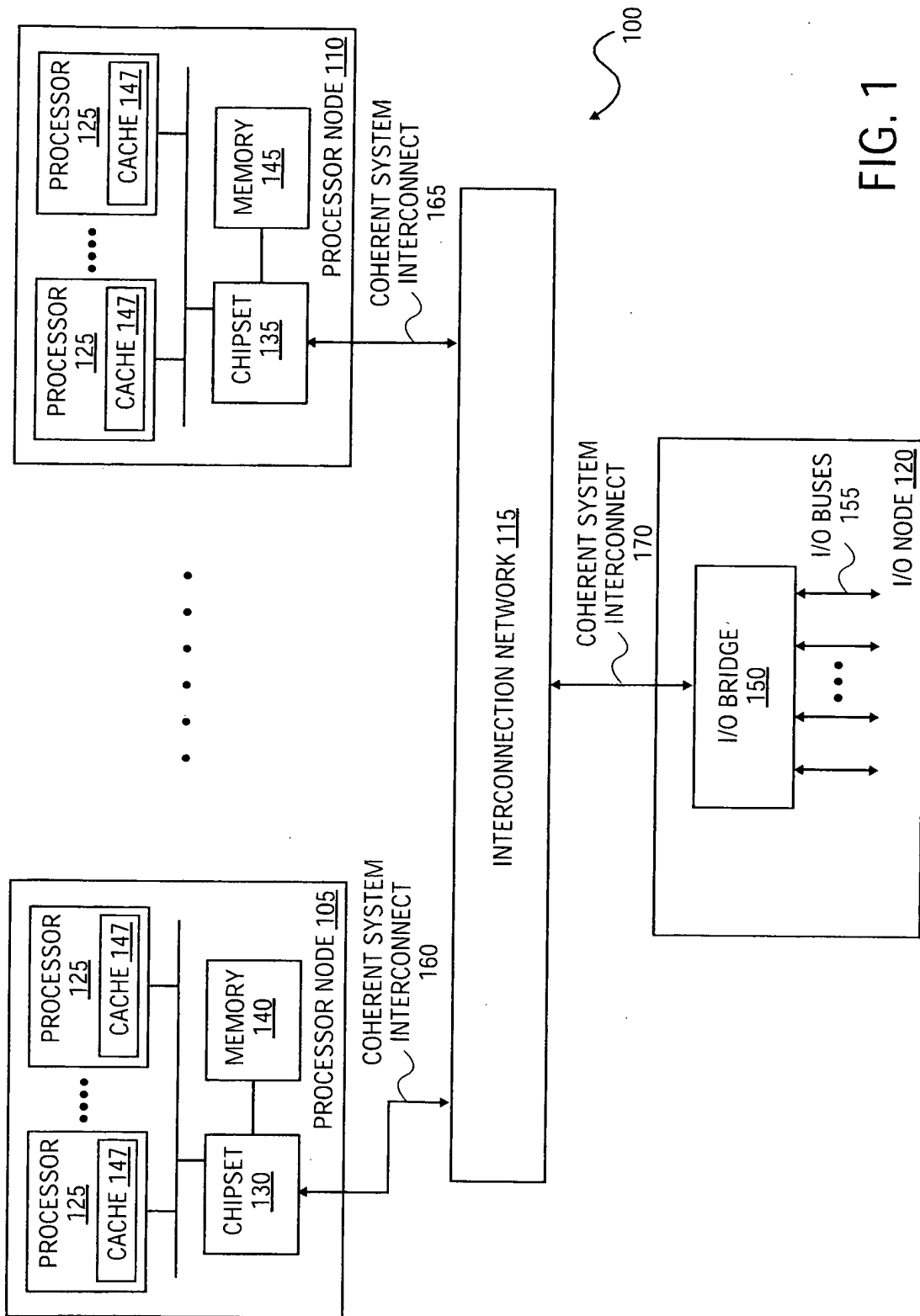Sheet 3 of 5
REPLACEMENT SHEET

BEGIN

SELECT COHERENT REQUEST FROM
I/O TRANSACTION REQUEST BUFFER — 305

310
READ
REQUEST OR WRITE
REQUEST?

WRITE

335
DOES
I/O CACHE BUFFER(S)
OWN EXCLUSIVE COPY
OF LINE?

Y

N

READ

315
IS
VALID COPY
OF REQUESTED LINE
IN I/O CACHE?

Y

N

ISSUE REQUEST TO
PREFETCH OWNERSHIP
OF LINE — 340

UPON RECEIVING SNOOP
RESPONSE, ALLOCATE
LINE IN EXCLUSIVE STATE
IN I/O CACHE BUFFER(S) — 345

ISSUE READ REQUEST FOR
NON-BINDING PREFETCH
OF REQUESTED LINE — 325

UPON RECEIVING REQUESTED
DATA, ALLOCATE DATA IN
SHARED STATE IN I/O
CACHE BUFFER(S) — 330

320
MORE
PENDNG REQUESTS
IN BUFFER?

Y

N

END

FIG. 3

"A METHOD AND APPARATUS FOR PIPELINING ORDERED INPUT/OUTPUT TRANSACTIONS TO
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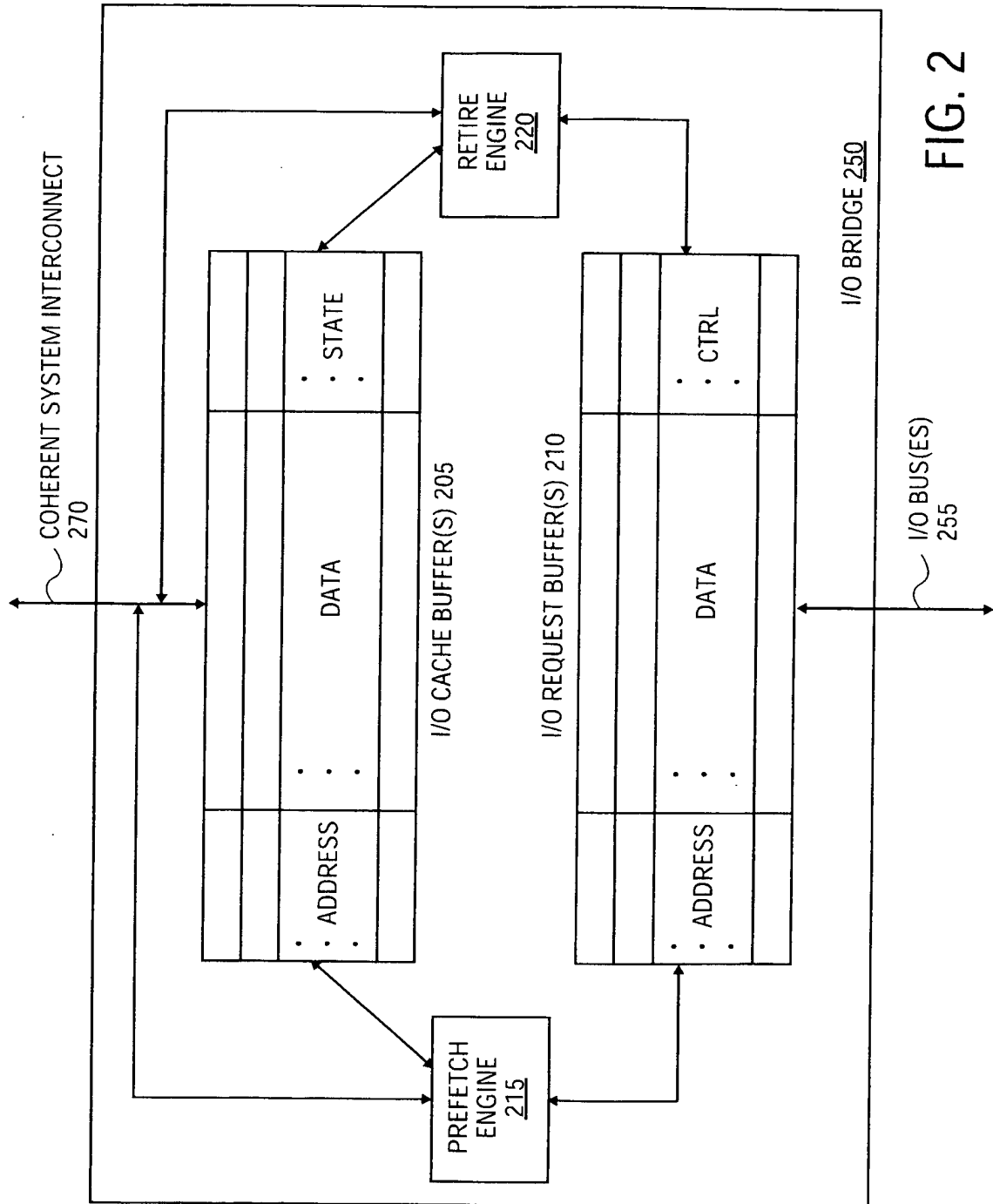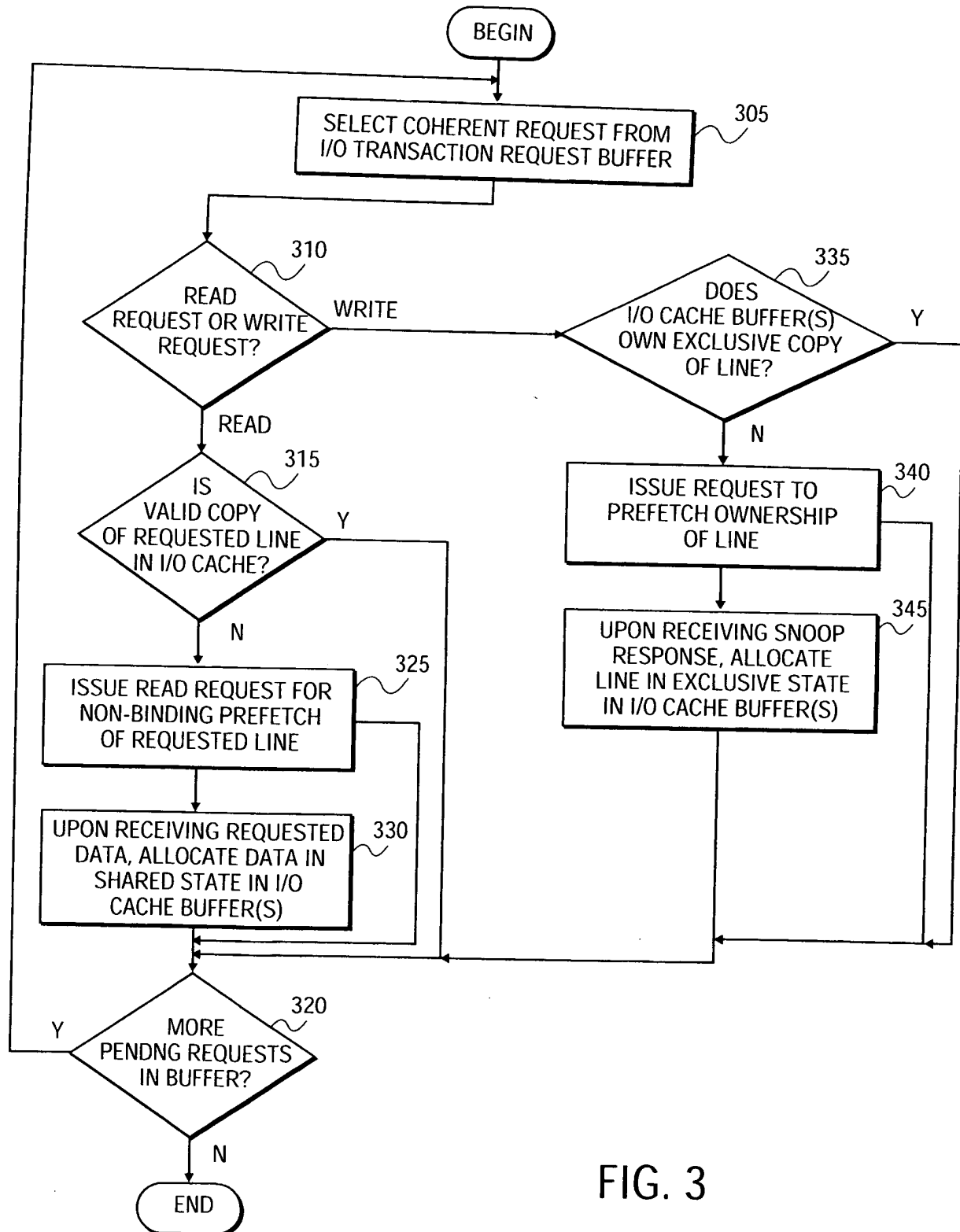Sheet 4 of 5
REPLACEMENT SHEET

FIG. 4

"A METHOD AND APPARATUS FOR PIPELINING ORDERED INPUT/OUTPUT TRANSACTIONS TO
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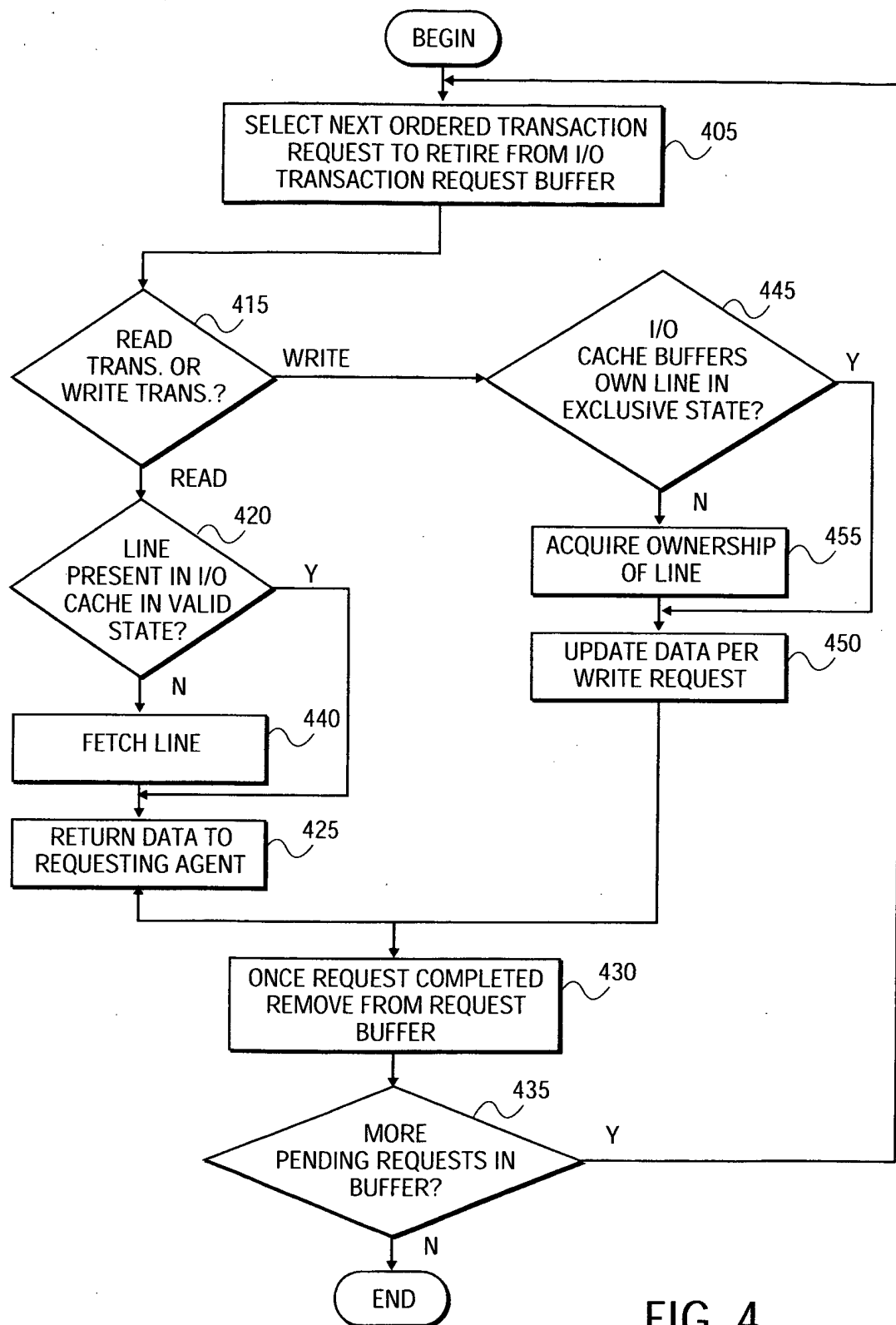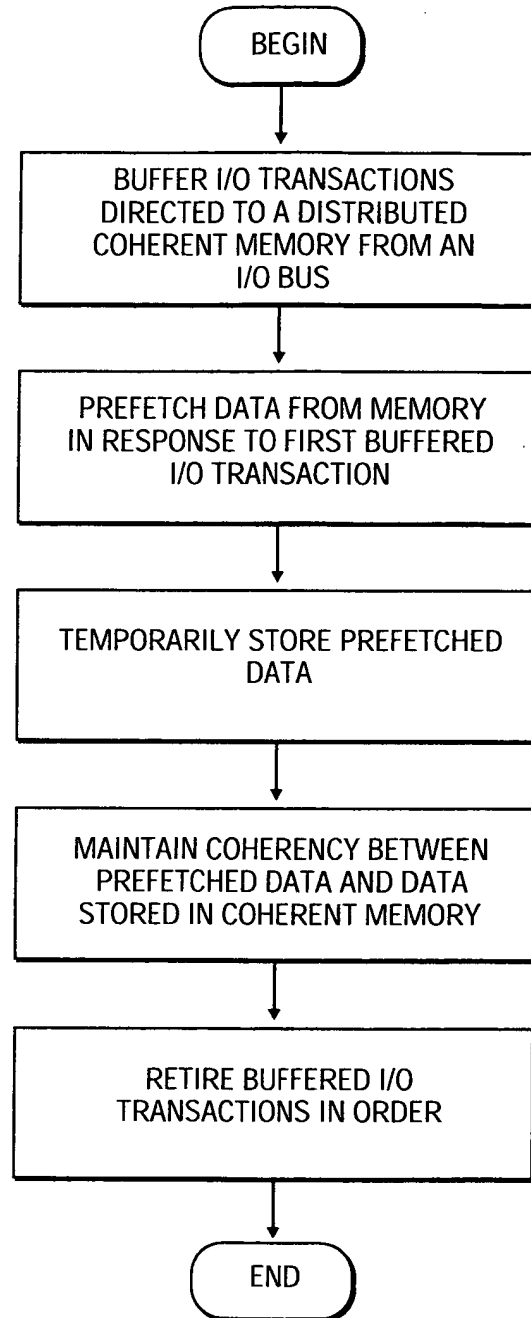Sheet 5 of 5
REPLACEMENT SHEET

BEGIN

BUFFER I/O TRANSACTIONS
DIRECTED TO A DISTRIBUTED
COHERENT MEMORY FROM AN
I/O BUS

PREFETCH DATA FROM MEMORY
IN RESPONSE TO FIRST BUFFERED
I/O TRANSACTION

TEMPORARILY STORE PREFETCHED
DATA

MAINTAIN COHERENCY BETWEEN
PREFETCHED DATA AND DATA
STORED IN COHERENT MEMORY

RETIRE BUFFERED I/O
TRANSACTIONS IN ORDER

END

FIG. 5